WHAT IS CLAIMED IS:

1. A content addressable memory having a function for extending a data width, comprising:

a plurality of memory blocks having a plurality of CAM words;

physical segments each including one or more memory blocks;

entry configuration set means for setting the number of CAM words which are combined to form one entry; and

a logical-segment-to-physical-segment converting circuit for converting logical segments constituting one entry to the physical segments according to the setting of said entry configuration set means.

2. A content addressable memory according to Claim 1, wherein said entry configuration set means is a register.

3. A content addressable memory according to Claim 2, wherein the register is a register having a bit width corresponding to the number of physical segments.

4. A content addressable memory according to Claim 1, wherein the CAM includes physical segments of which the number corresponds to the maximum number of words which are

combined.

5. A content addressable memory according to Claim 4, wherein said entry configuration set means is capable of setting the number of CAM words which is a divisor of the maximum number of words which are combined, where the divisor includes 1 and the maximum number of words which are combined.

6. A content addressable memory according to Claim 1, wherein the physical segments each comprise:

a search bit line;

a search bit line driver for driving the search bit line according to search data; and

a plurality of one-word circuits which store the data of one word and which search for a match between the stored data and the search data driven on the search bit line to output a match flag which is a match or mismatch search result.

7. A content addressable memory according to Claim 6, wherein, when said match is searched for, the search bit line only in a memory block in a search segment to be searched is driven by the search bit line driver.

8. A content addressable memory having a function for storing a plurality of entries composed of a combination of a plurality of words and searching the entries for each logical segment, comprising:

a plurality of memory blocks including a plurality of CAM words for storing the data of one word constituting the entries; and

physical segments each including one or more memory blocks, each physical segment including:

a search bit line;

a plurality of one-word circuits which search for a match between the data stored in the CAM word and search data driven on the search bit line to output a match flag which is a match or mismatch result; and

a search bit line driver for driving the search bit line according to the search data,

wherein, when said match is searched for, the search bit line only in a physical segment to be searched is driven by the search bit line driver.

9. A content addressable memory according to Claim 8, each of the physical segments further including a match flag control signal generating circuit for generating a match flag control signal which is a timing signal for capturing and holding a match flag output from the one-word circuit,

wherein, when said match is searched for, the match flag control signal only in a physical segment to be searched is generated.

10. A content addressable memory according to Claim 9, further comprising:

an entry configuration set register for setting the number of words which are combined to form the entries; and

a logical-segment-to-physical-segment converting circuit for converting a logical segment to be searched to a physical segment according to the setting of the entry configuration set register,

wherein one or a plurality of words are combined to form each of the entries.

11. A content addressable memory according to Claim 10, wherein each of the one-word circuits includes a CAM word having a plurality of CAM cells, and word logic for processing a match flag output from the CAM word;

the word logic includes a match flag register for holding the match flag, an AND chain having the match flags of the plurality of words coupled each other, and an entry match output circuit for outputting a match flag for the entries;

the word having the first address or the final address

in the plurality of words constituting each of the entries is the representative word of each corresponding entry;

if a word in each of the entries is not the representative word, an AND result of the match flags of said word and the previous word is output from the AND chain; and

if a word in each of the entries is the representative word, the AND chain is logically separated from the next word, and an AND result of the plurality of words constituting each corresponding entry is output as the entry match output from the entry match output.

12. A content addressable memory according to Claim 11, further comprising initialization means for initializing all the match flag registers to be in a match state before a first match search.

13. A content addressable memory according to Claim 12, wherein the CAM cells are mismatch-detection CAM cells for maintaining all the match flags in a physical segment not to be searched in the initial state or a match state and for capturing the match flags in the corresponding match flag registers.

14. A content addressable memory comprising:

a plurality of memory blocks having a plurality of one-word circuits;

physical segments each including one or more memory blocks;

entry configuration set means for setting the number of CAM words which are combined to form one entry;

a logical-segment-to-physical-segment converting circuit for converting logical segments constituting one entry to the physical segments according to the setting of said entry configuration set means; and

a word circuit chain having the maximum number of corresponding one-word circuits belonging to each physical block which are combined to form one entry, the one-word circuits being connected in series across the physical block.

15. A content addressable memory according to Claim 14, wherein each of the one-word circuits includes:

CAM words of m bits which store the data of one word and which search for a match between the stored data and search data to output a match or mismatch result to a match line;

a match flag for capturing and holding the match or mismatch result output to the match line at a predetermined timing;

an AND chain input;

an AND chain output for outputting an AND result between the AND chain input and the data held in the match flag or for outputting a signal always indicating a match according to a predetermined signal; and

an entry match output for outputting AND between the predetermined signal, and the AND result between the AND chain input and the data held in the match flag.

16. A content addressable memory according to Claim 15, wherein the predetermined timing is a point when search operation is completed, when a physical block to which the one-word circuit belongs is to be searched, and the predetermined signal is an entry representative physical segment instruction signal.